In The Claims:

Claims 1-44 (canceled).

45. (currently amended) An electronic structure comprising:

a conductive pad on a substrate;

~~a insulating~~ an insulating layer on the substrate and on the conductive pad, the insulating layer having a via therein so that a portion of the conductive pad opposite the substrate is free of the insulating layer;

a seed layer on the portion of the conductive pad free of the insulating layer, on sidewalls of the via, and on a surface of the insulating layer opposite the substrate;

a conductive shunt layer on the portion of the conductive pad free of the insulating layer, on sidewalls of the via, and on surface portions of the insulating layer surrounding the via opposite the substrate and the conductive pad, wherein the conductive shunt layer has a thickness of at least approximately 0.5μm and wherein the conductive shunt layer comprises copper and wherein the seed layer is between the conductive shunt layer and the insulating layer and between the conductive shunt layer and the conductive pad;

a conductive barrier layer on the conductive shunt layer wherein the conductive barrier layer comprises at least one of nickel, platinum, palladium, and/or combinations thereof; and

a solder layer on the conductive ~~shunt layer~~ barrier layer wherein the conductive shunt layer and the solder layer comprise different materials, wherein the conductive barrier layer is between the conductive shunt layer and the solder layer, wherein the conductive shunt layer, the conductive barrier layer, and the solder layer are on portions of the seed layer, and wherein portions of the seed layer are free of the conductive shunt layer, the conductive barrier layer, and the solder layer.

46. (original) An electronic structure according to Claim 45 wherein the solder layer has a rounded surface opposite the conductive shunt layer having the thickness of at least approximately 0.5μm.

47. (currently amended) ~~An electronic structure according to Claim 45~~ An electronic structure comprising:

a conductive pad on a substrate;

an insulating layer on the substrate and on the conductive pad, the insulating layer having a via therein so that a portion of the conductive pad opposite the substrate is free of the insulating layer;

a conductive shunt layer on the portion of the conductive pad free of the insulating layer, on sidewalls of the via, and on surface portions of the insulating layer surrounding the via opposite the substrate and the conductive pad, wherein the conductive shunt layer has a thickness of at least approximately 1.0μm and wherein the conductive shunt layer comprises copper;

a conductive barrier layer on the conductive shunt layer wherein the conductive barrier layer comprises at least one of nickel, platinum, palladium, and/or combinations thereof; and

a solder layer on the conductive barrier layer, wherein the conductive shunt layer and the solder layer comprise different materials and wherein the conductive barrier layer is between the conductive shunt layer and the solder layer.

48. (original) An electronic structure according to Claim 45 wherein the conductive shunt layer has a thickness in the range of approximately 1.0μm to 5.0μm.

Claim 49 (canceled).

50. (currently amended) An electronic structure according to ~~Claim 45~~ Claim 47 further comprising:

a seed layer between the conductive shunt layer and the conductive pad and between the conductive shunt layer and the insulating layer.

51. (original) An electronic structure according to Claim 50 wherein the seed layer comprises an adhesion layer of a material different than that of the conductive shunt layer.

52. (original) An electronic structure according to Claim 51 wherein the adhesion layer comprises titanium, tungsten, chrome, and/or combinations thereof.

53. (original) An electronic structure according to Claim 51 wherein the seed layer comprises a plating conduction layer on the adhesion layer opposite the substrate, wherein the plating conduction layer and the conductive shunt layer comprise a common material.

54. (original) An electronic structure according to Claim 50 wherein the conductive shunt layer, the conductive barrier layer, and the solder layer are on portions of the seed layer, and wherein portions of the seed layer are free of the conductive shunt layer, the conductive barrier layer, and the solder layer.

Claims 55-56 (canceled).

57. (original) An electronic structure according to Claim 45 further comprising:

a primary conductive trace on the substrate so that the primary conductive trace is between the substrate and the insulating layer; and

an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing at least two separate current flow paths between the primary conductive trace and the conductive pad.

Claims 58-93 (canceled).

94. (previously presented) An electronic structure according to Claim 45 further comprising:

a conductive barrier layer on the conductive shunt layer opposite the conductive pad and the insulating layer wherein the conductive barrier layer comprises at least one of nickel, palladium, platinum, and/or combinations thereof, wherein the solder layer and the barrier layer comprise different materials.

Claims 95-96 (canceled).

97. (previously presented) An electronic structure according to Claim 94 wherein the conductive shunt layer comprises a layer of copper having a thickness of at least approximately 0.5μm.

98. (new) An electronic structure according to Claim 45 wherein the seed layer comprises an adhesion layer of a material different than that of the conductive shunt layer.

99. (new) An electronic structure according to Claim 98 wherein the adhesion layer comprises titanium, tungsten, chrome, and/or combinations thereof.

100. (new) An electronic structure according to Claim 98 wherein the seed layer comprises a plating conduction layer on the adhesion layer opposite the substrate, wherein the plating conduction layer and the conductive shunt layer comprise a common material.

101. (new) An electronic structure according to Claim 45 wherein the conductive shunt layer has a thickness of at least approximately 1.0μm.

102. (new) An electronic structure according to Claim 47 wherein the conductive shunt layer has a thickness in the range of approximately 1.0μm to 5.0μm.

103. (new) An electronic structure according to Claim 47 further comprising:

a primary conductive trace on the substrate so that the primary conductive trace is between the substrate and the insulating layer; and

an electrical coupling between the primary conductive trace and the conductive pad, the electrical coupling providing at least two separate current flow paths between the primary conductive trace and the conductive pad.